What is claimed is:

1. A semiconductor device, comprising:

a power supply circuit that comprises:

a first power supply terminal supplying a first operating voltage and a second power supply terminal supplying a second operating voltage lower than said first operating voltage;

a first field effect transistor in which a source-drain path is connected in series between said first power supply terminal and an output terminal; and

a second field effect transistor in which a source-drain path is connected in series between said output terminal and said second power supply terminal,

wherein said first field effect transistor includes:

a semiconductor substrate having a first main surface and a second main surface opposite to said first main surface;

a gate electrode formed on said first main surface of the semiconductor substrate via a gate insulating film;

a source region and a drain region having a first conductive type formed on said first main surface and on both end portions of said gate electrode; and

a semiconductor region for forming a channel formed on said first main surface and between said source region and said drain region, the semiconductor region for forming a channel having a second conductive type which is reverse to said first conductive type, and

wherein said second field effect transistor includes:

a semiconductor substrate having a first main surface

and a second main surface opposite to said first main surface;

a gate electrode formed on said first main surface of the semiconductor substrate via a gate insulating film;

a semiconductor region for forming a channel having the second conductive type, which is formed on said first main surface and a part of which overlaps said gate electrode in two dimensions;

a source region having the first conductive type, which is formed in said semiconductor region for forming a channel and formed on one end portion of said gate electrode; and

a drain region formed on said second main surface and formed under said semiconductor region for forming a channel.

2. The semiconductor device according to claim 1,

wherein a source of said first field effect transistor and a drain of said second field effect transistor are joined to a common conductor and are electrically connected to each other.

3. The semiconductor device according to claim 2,

wherein said first field effect transistor and said second field effect transistor are sealed in the same package.

4. The semiconductor device according to claim 1,

wherein an outer terminal for a gate and an outer terminal for a drain are provided on a first main surface of a semiconductor chip on which said first field effect transistor is formed, and an outer terminal for a source is provided on a second main surface opposite to said first main surface.

5. The semiconductor device according to claim 4,

wherein said first field effect transistor has a

structure in which a semiconductor region for a source formed on said first main surface is electrically connected to said outer terminal for a source provided on said second main surface.

6. The semiconductor device according to claim 5,

wherein said first field effect transistor includes: the semiconductor region for a source formed on said first main surface; a semiconductor region for a drain formed on said first main surface; a gate insulating film formed on said first main surface between said semiconductor regions; a gate electrode formed on said gate insulating film; a conductor film formed on said first main surface and electrically connected to said semiconductor region for a source; a semiconductor region formed on said semiconductor chip and functioning to electrically connect said conductor film to said outer terminal for a source; an insulating film deposited so as to cover said gate electrode and said conductor film on said first main surface; said outer terminal for a gate provided on said insulating film and electrically connected to said gate electrode; and said outer terminal for a drain provided on said insulating film and electrically connected to said semiconductor region for a drain.

7. The semiconductor device according to claim 6,

wherein said outer terminal for a gate and said outer terminal for a drain arranged on said first surface are electrically connected to leads of a package using bonding wires.

8. The semiconductor device according to claim 6,

wherein said outer terminal for a gate and said outer terminal for a drain arranged on said first surface are electrically connected to leads of a package using bump electrodes.

9. The semiconductor device according to claim 1,

wherein said second field effect transistor has a trench gate electrode structure in which a gate electrode is provided in a trench dug in a direction cross to a first main surface of a semiconductor chip.

10. A semiconductor device, comprising:

a first terminal for supplying a first potential;

a first field effect transistor having a drain connected to said first terminal;

a second field effect transistor having a drain electrically connected to a source of said first field effect transistor; and

a second terminal for supplying a potential lower than said first potential and to which a source of said second field effect transistor is electrically connected,

wherein said first field effect transistor is constituted of a horizontal field effect transistor and said second field effect transistor is constituted of a vertical field effect transistor.

11. The semiconductor device according to claim 10,

wherein the source of said first field effect transistor and a drain of said second field effect transistor are joined to a common conductor and are electrically connected to each other.

12. The semiconductor device according to claim 10,

wherein said first field effect transistor and said second field effect transistor are sealed in the same package.

13. The semiconductor device according to claim 10,

wherein an outer terminal for a gate and an outer terminal for a drain are provided on a first surface of a semiconductor chip on which said first field effect transistor is formed, and an outer terminal for a source is provided on a second surface of said semiconductor chip opposite to said first surface.

14. The semiconductor device according to claim 13,

wherein said first field effect transistor has a structure in which a semiconductor region for a source formed on said first surface is electrically connected to said outer terminal for a source provided on said second surface.

15. The semiconductor device according to claim 10, further comprising a power supply circuit which comprises a pulse width modulation circuit connected to gates of said first and second field effect transistors; a coil connected to outputs of said first and second field effect transistors; and a capacitor connected in parallel to said first and second field effect transistors in a subsequent stage of said coil.

16. A semiconductor device comprising:

a semiconductor region for a source formed on a first surface of a semiconductor chip;

a semiconductor region for a drain formed on said first surface;

a gate insulating film formed on said first surface

between said semiconductor region for a source and said semiconductor region for a drain;

a gate electrode formed on said gate insulating film;

an insulating film deposited so as to cover said gate electrode on said first surface;

an outer terminal for a gate provided on said insulating film and electrically connected to said gate electrode;

an outer terminal for a drain provided on said insulating film and electrically connected to said semiconductor region for a drain;

an outer terminal for a source formed on a second surface opposite of said semiconductor chip to said first surface; and

connection means for electrically connecting said semiconductor region for a source on said first surface to said outer terminal for a source.

17. The semiconductor device according to claim 16,

wherein said connection means comprises a conductor film formed on said first surface and electrically connected to said semiconductor region for a source; and a semiconductor region formed on said semiconductor chip so as to connect said conductor film to the outer terminal for a source.

18. A semiconductor device, comprising:

a first semiconductor chip on which a first field effect transistor of a first capacitance is formed; and

a second semiconductor chip on which a second field effect transistor of a second capacitance different from said

first capacitance is formed,

wherein an outer terminal for a source is provided on a rear surface of said first semiconductor chip; an outer terminal for a drain is provided on a rear surface of said second semiconductor chip; and the rear surfaces of said first and second semiconductor chips are joined to the same conductor, thereby electrically connecting a source of said first field effect transistor to a drain of said second field effect transistor.